The Crusoe Microprocessor for Mobile Platforms

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TRANSMETA Corporation

Platform 2000

Overview

- 400MHz TM3120 VLIW Processor
- 700MHz TM5400 VLIW Processor
- Low power
- 4 micro-ops per cycle
- Large caches
- Software approach ("Code Morphing")
- Runs standard x86 operating systems, BIOS's, and applications

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Transmeta Vision – How it Began

1980: RISC idea –
simple fast chips, but recompile applications

1995: Complexity growing
- RISC processors no longer simple
- x86 processors never were

Big, complex chips

Chips are hot – approaching 100 Watts

Backwards compatibility baggage

Time to re-think the microprocessor

The Processor Industry's Problem

The two big problems:
- Complexity of all-silicon solutions
- Compatibility with x86 PC software

Transmeta's solution was not to use silicon, but software.

Transmeta's Vision: A Software Based Microprocessor

Idea: Software could be integral to a microprocessor

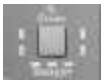
A combined hardware/software solution:

- **Simpler hardware, thus cheaper and cooler**
- **Easier to design and debug**
- **No worry about backward compatibility in hardware**
- **Software could LEARN– the first SMART processor**

Crusoe
is the first
microprocessor
whose instruction set
is implemented entirely with
Software.

Crusoe Technology and Benefits

Crusoe is

Code Morphing Software +  = x86 Compatibility

3/4 + 1/4

Low Power

PC Performance

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Crusoe Spans A Complete Range of Mobile Computers

Crusoe in Mobile Internet Computers

Mobile Client | Web pad | Thin+Light Mobile PC | Full Featured Mobile PC

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The First Two Crusoe Processors

TM5400

Lightweight Notebook Computers
Microsoft Windows

700 MHz
400 KBytes of cache
1 Watt
x86 compatible

TM3120

Mobile Internet Appliances
Mobile Linux

400 MHz
108 KBytes of cache
1 Watt
x86 compatible

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Crusoe is Fully Internet Compatible

Crusoe:

- **100% x86 compatible**
- **Supports full PC system architecture**
- **Runs all x86 operating systems**
- **Runs browser AND its x86 plug-ins**

For the Full Internet Experience

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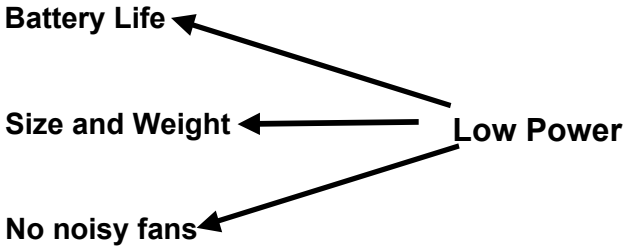
Crusoe Advantages for Mobile Computing



Full Internet Compatibility

Performance on Demand

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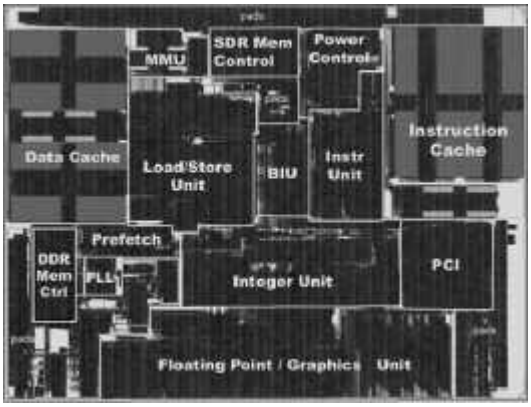
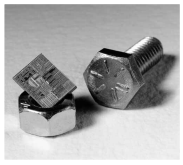
TM3120 for Mobile Internet Devices (With Mobile Linux O/S)





	TM3120
Frequency Range	366-400 MHz
L1 Cache	96KB
L2Cache	
Main Memory	SDRAM
Upgrade memory	
North Bridge	Integrated
Package	474 BGA
Fab Partner	IBM
Process Technology	.22u
Die Size	77mm
Sample	Now
Production	Now

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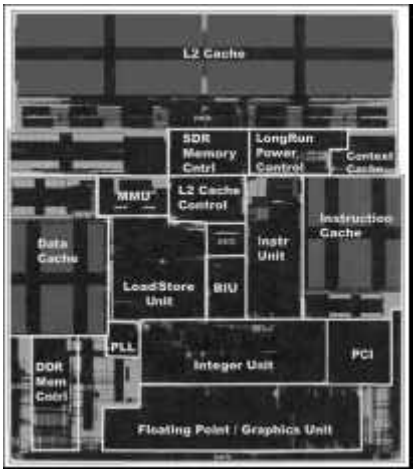
TM5400 for Ultra-Light PCs (With Microsoft O/S)



	TM5400
Frequency Range	600-700 MHz
L1 Cache	128K
L2Cache	256K
Main Memory	DDR-SDRAM
Upgrade memory	SDRAM
North Bridge	Integrated
Package	474 BGA
Fab Partner	IBM
Process Technology	.18u
Die Size	73mm
Sample	Now
Production	Mid 2000

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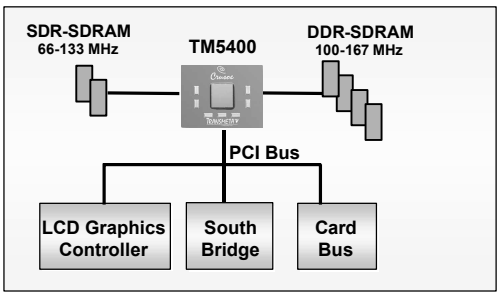
Crusoe Processor Hardware System Diagram

Uses standard PC components:

- **SDRAM and DDR-SDRAM memory**
- **PCI standard I/O devices and controllers**
- **Improved system architecture for better performance & lower power**



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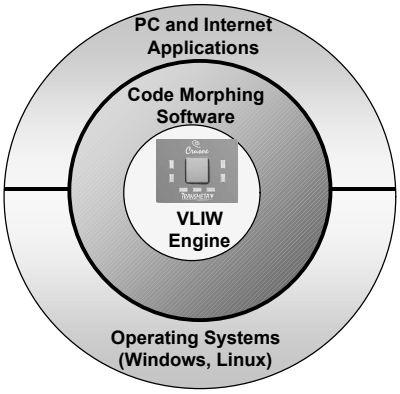
The Smart Microprocessor Architecture



- 100% x86 compatible
- High speed, low power VLIW engine
- "Morphs" x86 to VLIW
- VLIW + Code Morphing = x86 compatible solution

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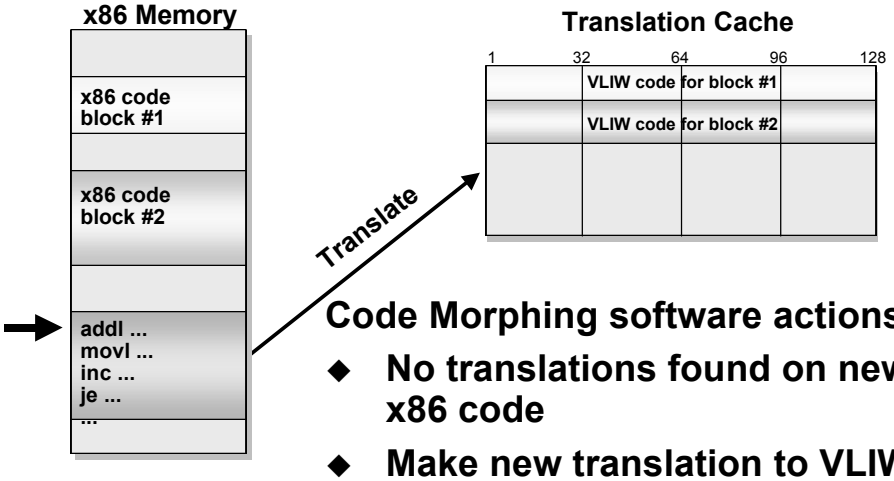
Translation of x86 instructions to VLIW



Code Morphing software actions

- No translations found on new x86 code
- Make new translation to VLIW

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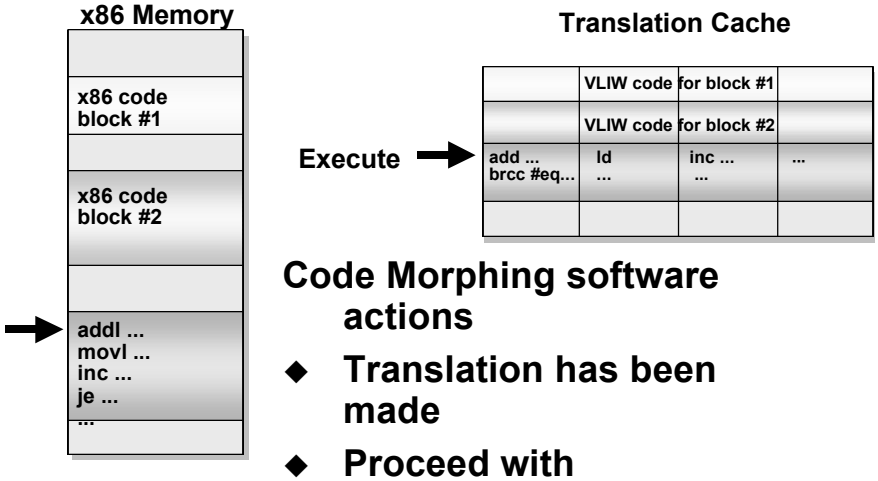
Dynamic Software Execution



Code Morphing software actions

- Translation has been made
- Proceed with execution

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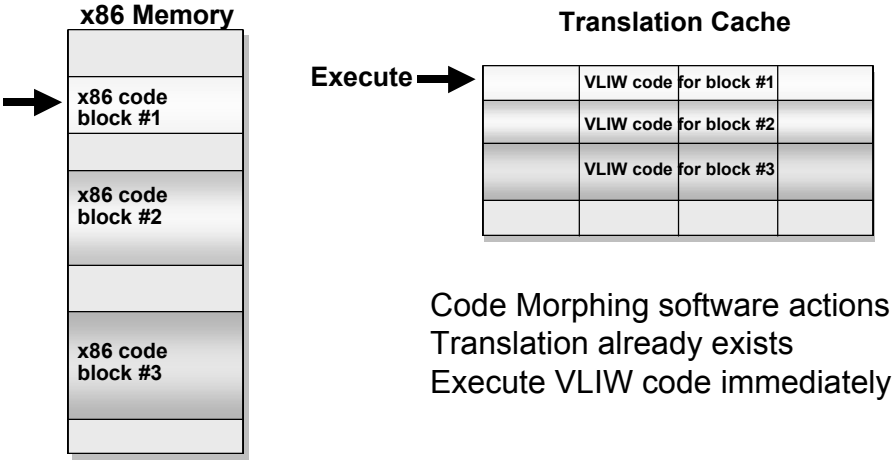
Dynamic Software Execution (2nd Pass)



Code Morphing software actions
Translation already exists
Execute VLIW code immediately

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Code Morphing Process

- Gather execution statistics
- X86 Decode
- Crusoe atom (aka micro-op) generation
- Atom scheduling (Atoms -> Molecules)
- Cache sequences of molecules (translations)
- Execute translations
- Monitor execution and retranslate if opportunity exists for higher performance

Special Hardware Support

- Shadowed register file supports aggressive scheduling
- Gated store buffer gives additional scheduling freedom
- Alias hardware supports reordering and eliminating memory operations
- T-bit: memory protection to ensure translation cache consistency

Shadowed Register File

- 64 general purpose 32-bit registers
- 48 of these have shadow copies
- Commit atom copies working -> shadow
- Roll-back atom copies shadow -> working
- Commits issued when x86 state is consistent
- Roll-backs used for exceptions

Gated Store Buffer

- Holds 31 values destined for memory
- Values come from store atoms
- Snooped by subsequent load atoms
- Values go to memory on commit
- Values are discarded on roll-back
- Allows stores to preceed atoms which can fault
- Essential for good performance because allows longer translations and scheduling freedom

Alias Hardware

- 8 alias registers watch memory traffic
- Load and store atoms can set alias registers
- Allows loads to pass stores
- Exception occurs if speculation is incorrect
- Software recovers

T-bit Hardware

- Handles self modifying code
- Per-physical-page bit in TLB
- Like a write-protect bit
- Set on x86 pages with translated instructions
- Translations reevaluated on T-bit fault
- Part of Transmeta's translation-cache consistency mechanisms

Crusoe Processor Software Optimization

x86 (IA-32) Instruction Mix

```
      1. movl   %ecx,$0x3
      2. jmp    lbl1
lbl1:
      3. movl   %edx,0x2fc(%ebp)
      4. movl   %eax,0x304(%ebp)
      5. movl   %esi,$0x0
      6. cmpl   %edx,%eax
      7. movl   0x40(%esp,1),$0x0
      8. jle    skip1
      9. movl   %esi,$0x1
skip1:
     10. movl   0x6c(%esp,1),%esi
     11. cmpl   %edx,%eax
     12. movl   %eax,$0x1
     13. jl     skip2
     14. xorl   %eax,%eax
skip2:
     15. movl   %esi,0x308(%ebp)
     16. movl   %edi,0x300(%ebp)
     17. movl   0x7c(%esp,1),%eax
     18. cmpl   %esi,%edi
     19. movl   %eax,$0x0
     20. jnl    exit1
exit2:
```

"Morphed" (128-bit) VLIW Instructions

```
 1. addi %r39,%ebp,0x2fc
 2. addi %r38,%ebp,0x304
 3. ld %edx,[%r39];      add %r27,%r38,4;     add %r26,%r38,-4
 4. ld %r31,[%r38];      add %r35,0,1;        add %r36,%esp,0x40
 5. ldp %esi,[%r27];     add %r33,%esp,0x6c;  sub.c %null,%edx,%r31
 6. ldp %edi,[%r26];     sel #le %r32,0,%r35;
 7. stam 0,[%r36];       sel #l %r24,%r35,0;  add %r25,%esp,0x7c
 8. stam %r32,[%r33];    add %ecx,0,3;        sub.c %null,%esi,%edi
 9. st %r24,[%r25];      or %eax,0,0;         brcc #lt,<exit2>
10. br <exit1>
```

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Crusoe Advantages

- Low power
- High performance
- 100% compatabile with x86 software
- Integrated northbridge
- Upgradable over the Internet

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Transmeta Technology

- Moving hardware/software line allows clean, fast, small silicon AND x86 compatability
- Design, debug, verification of hardware and software in parallel
- Much higher verification bandwidth for software component
- Can attack performance with hardware AND software improvements

Question & Answer Session